

[4240] - 102
M.C.A. - I (Under Science Faculty)
COMPUTER SCIENCE
CS - 102 : Computer Architecture
(2008 Pattern) (Sem. - I)

Time : 3 Hours]

[Max. Marks :80

Instructions to the candidates:

- 1) All questions are compulsory.*
- 2) Figures to the right indicate full marks.*
- 3) All questions carry equal marks.*
- 4) Draw neat diagrams wherever necessary.*

Q1) Attempt any four of the following : **[4 × 4 = 16]**

- a) What is Half adder? How is it used to design full adder circuit?
- b) What does 'VESA' stands for, in Computer bus structure? State its features.
- c) Draw logic diagram of 2:4 Decoder and explain its working.
- d) Explain with suitable example 'Instruction Cycle' in Microprocessor.
- e) Explain 4 bit binary weighted digital to analog converter.

Q2) Attempt any two of the following : **[2 × 8 = 16]**

- a) Explain registers of 64 bit Intel Microprocessor with neat block diagram.
- b) Explain following operations of shift register using D-filp-flop.
 - i) Serial In Serial Out.
 - ii) Serial In Parallel Out.
 - iii) Parallel In Serial Out.
 - iv) Parallel In Parallel Out.
- c) Explain with neat diagram, 3 bit flash ADC,

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